

FIG. 1A

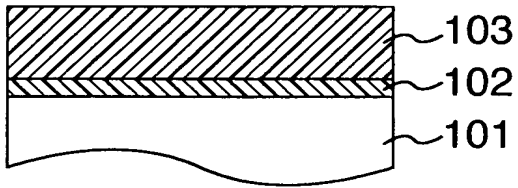


FIG. 1B

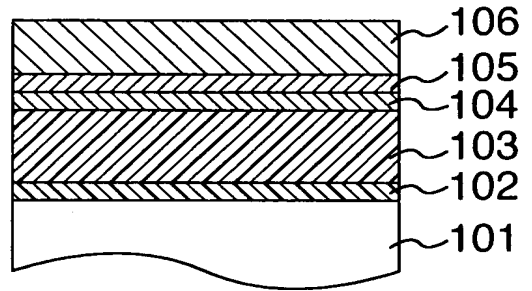


FIG. 1C

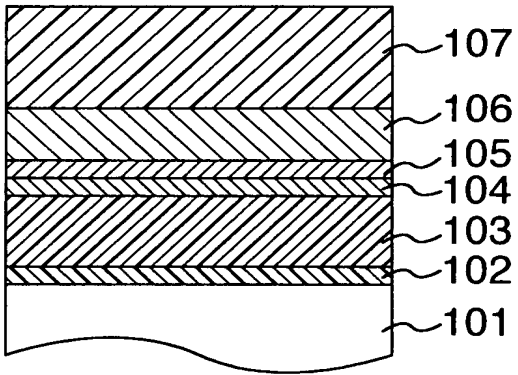


FIG. 1D

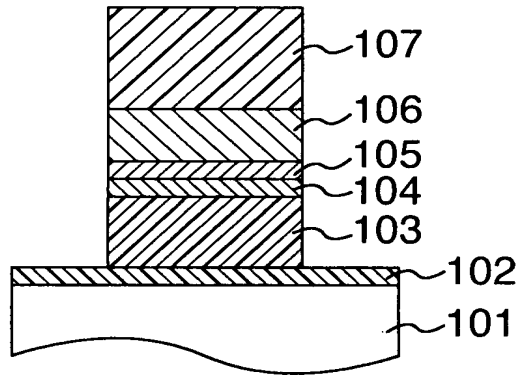


FIG. 1E

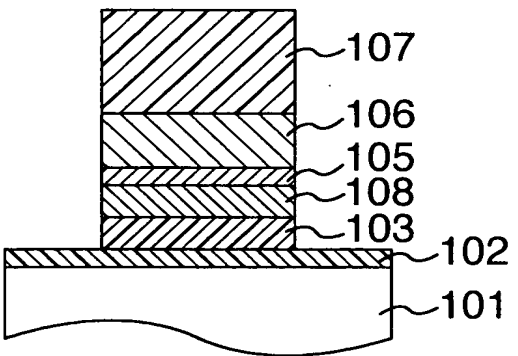


FIG. 2A

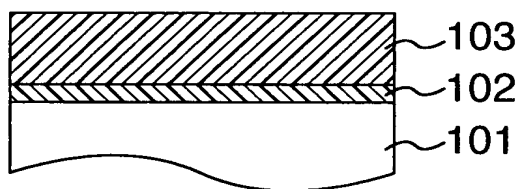


FIG. 2B

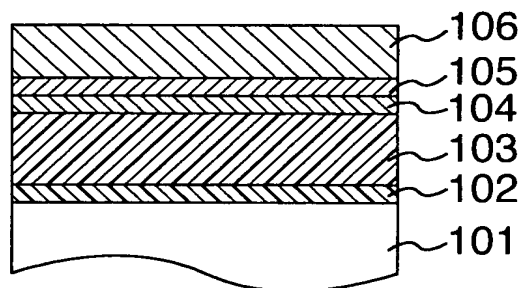


FIG. 2C

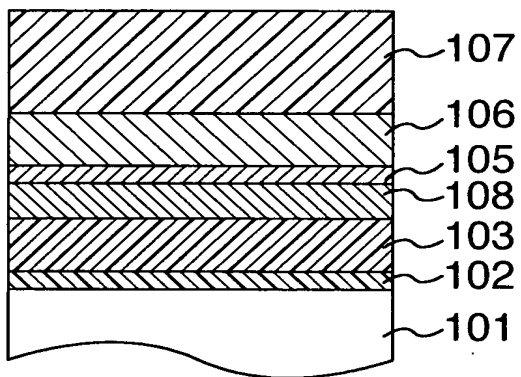


FIG. 2D

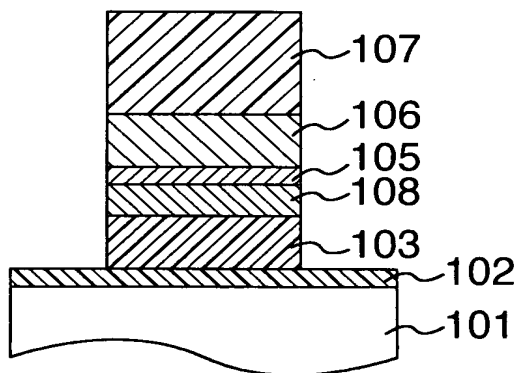


FIG. 3A

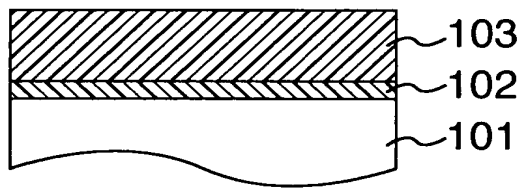


FIG. 3B

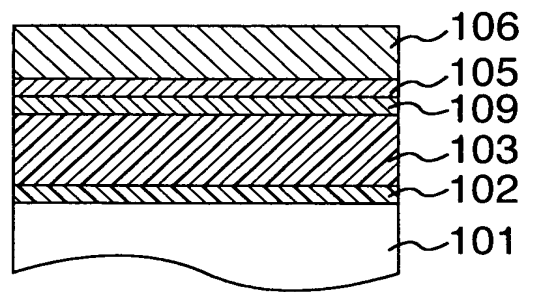


FIG. 3C

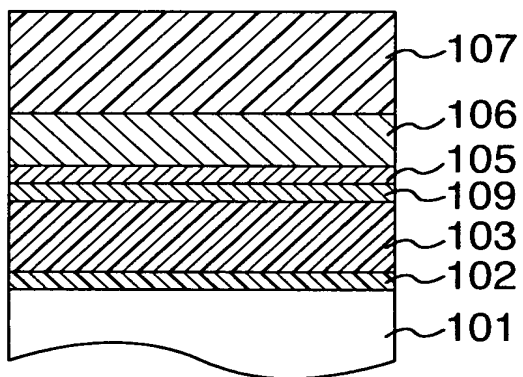


FIG. 3D

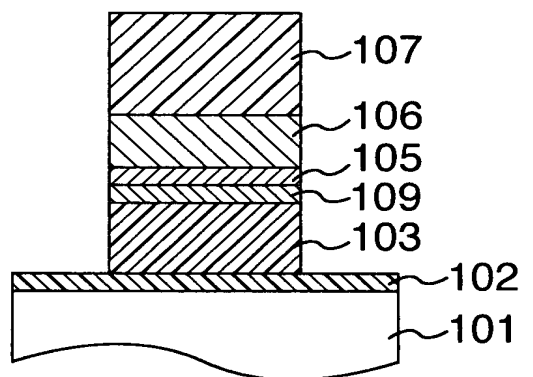


FIG. 4A

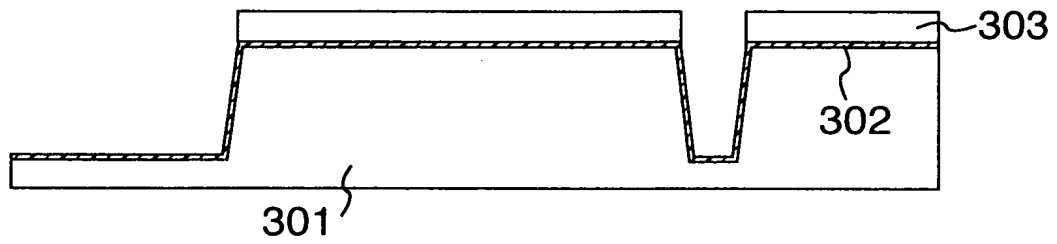


FIG. 4B

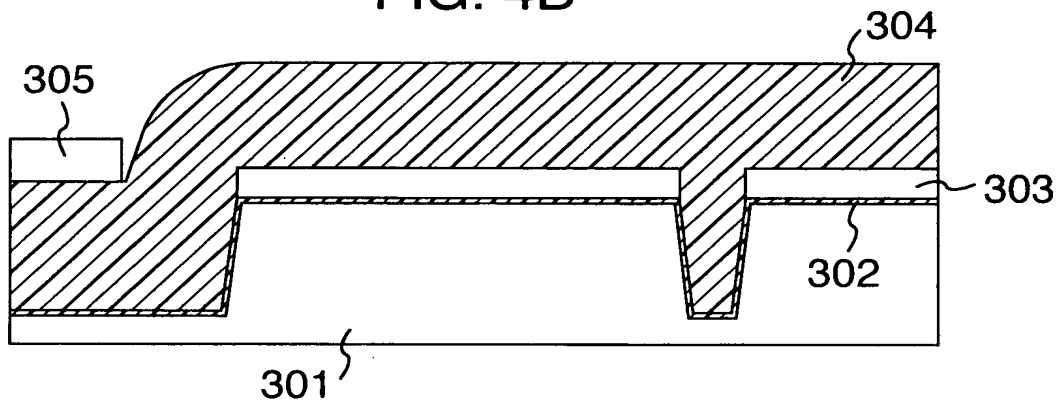
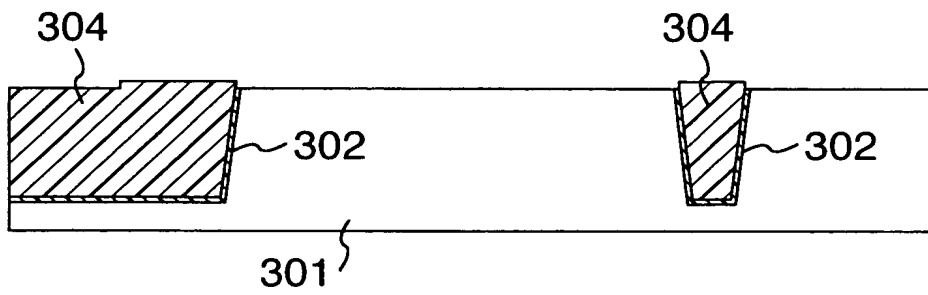
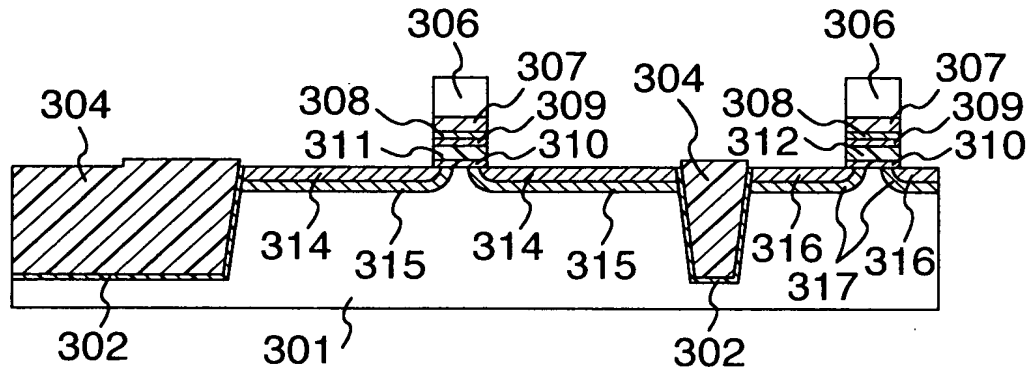


FIG. 4C



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100



This cross-sectional view shows a semiconductor device with a substrate 301. A base layer 302 is formed on the substrate. Two active regions are defined by side walls 304. Each active region contains a stack of layers: a bottom layer 311, a middle layer 312, and a top layer 313. A central layer 314 is located between the two active regions. A contact layer 315 is formed on the top layer 313. A contact pad 316 is formed on the contact layer 315. A contact wire 317 is formed on the contact pad 316. A contact pad 318 is formed on the contact layer 315. A contact wire 319 is formed on the contact pad 318. A contact pad 319 is formed on the contact layer 315. A contact wire 319 is formed on the contact pad 318.

This cross-sectional view shows a semiconductor device with a substrate 301. A base layer 302 is formed on the substrate. Two active regions are defined by isolation regions 304. Each active region contains a gate stack 313 (gate oxide 306, gate electrode 307) and a source/drain region 310. The source/drain region is formed by a conductive layer 311 and a dielectric layer 312. The device is surrounded by a protective layer 314 and a passivation layer 315. The top surface is covered by a layer 316, which is patterned into a grid-like structure 317. The bottom surface of the substrate is labeled 318.

FIG. 6A

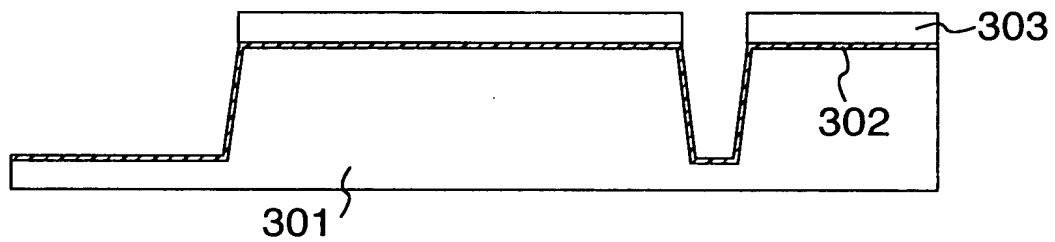


FIG. 6B

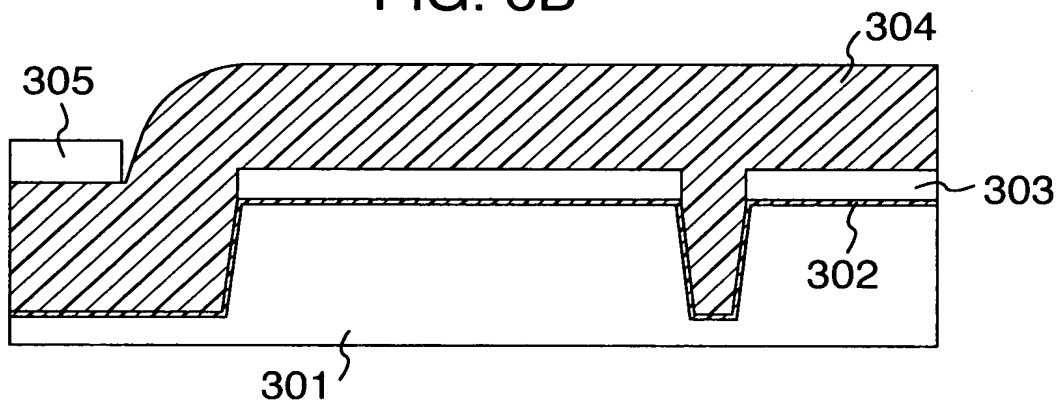


FIG. 6C

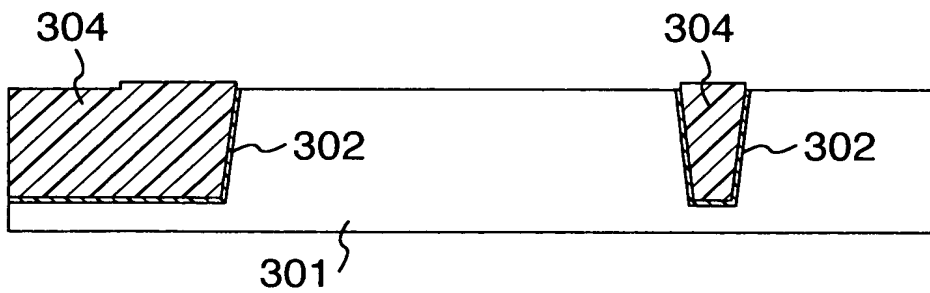


FIG. 7A

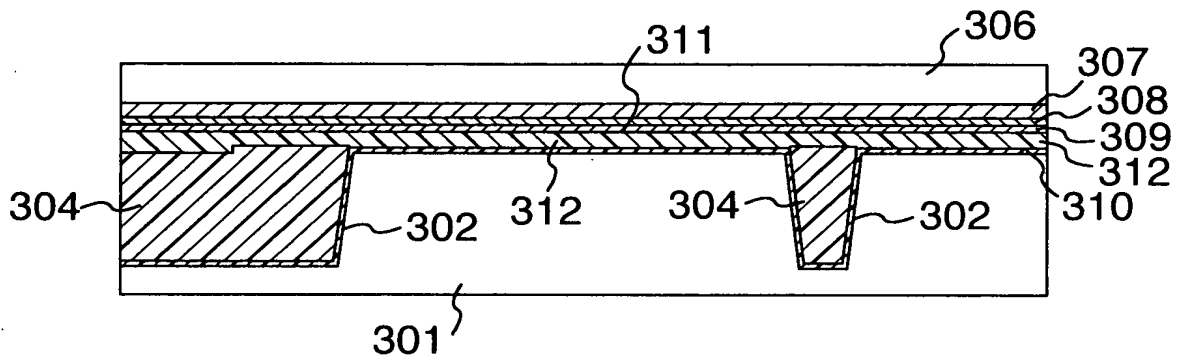


FIG. 7B

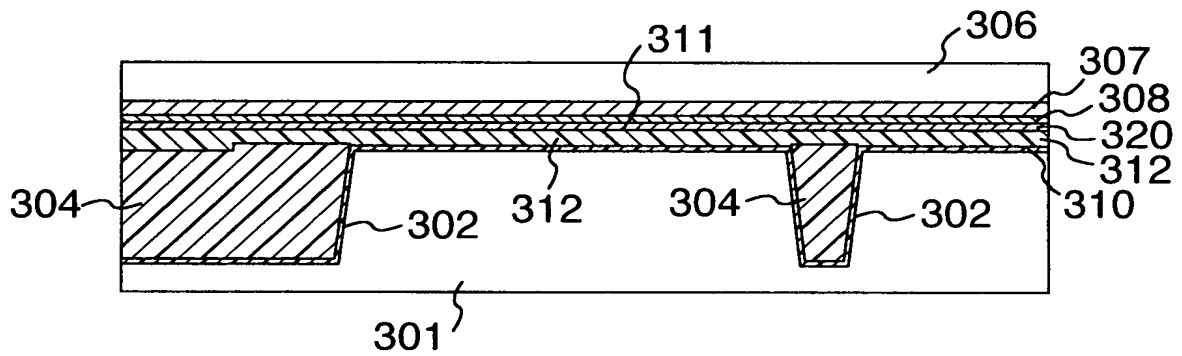


FIG. 7C

